COMPUTER-AIDED INSPECTION OF SOME TOPOLOGICAL Rules OF INTEGRATED CIRCUIT LAYERS

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Abstract. The visual inspection algorithms for verification of industrial topological rules of integrated circuits are proposed. The algorithms include segmentation of images of topological layer with subsequent extraction of typical patterns on these images for defects localization. The unique feature of the technology is that the inspection of the design technological rules is performed at different stages of processing. Thus a time-consuming procedure of image matching with the purpose of localization of defects is performed only for some images from the whole image set. The inspection algorithms are included at the system of topological layers processing, which is applied both for topology reconstruction of integrated circuits and for the inspection of its manufacture.

Introduction

The development of any kind of operative analysis systems providing image registration, visual information processing and interpretation is the actual practical task. The visual or optical inspection of integrated circuits in cooperative with another types of inspection, such as X-ray or ultrasonic, is the important part of a modern production. Therefore in this paper the main attention is given to image analysis algorithms and algorithms of defects detection which were developed for processing metal layers of integrated circuits.

Two main approaches for optical inspection are known: pattern matching (in this case the template usually is obtained from CAD); verification of design technological rules [1]. Above approaches are combined in the proposed processing technology, but the time-consuming procedure of image matching with the purpose of localization of defects is performed for additional analysis only for some fragments of the whole image. The inspection objects are integrated circuit (IC) or its photo mask set presented as a collection of gray-scale or colour fragments. The computer-aided system of digital image processing, in which the proposed algorithms are used, presents oneself the decision support system. It provides reconstruction of the topology of metallization layers of IC (further - object) in the interactive mode by using digitized images of the object, with subsequent definition and localization of a different type of faults.

The image processing consists of graphic data reduction and enhancement exploring discrete two-dimensional Walsh and Haar functions, extraction of typical elements with specified characteristics on the base of Hough transform, which allows to describe extracted objects with a given degree of accuracy by straight-line segments of different length, detection of defects and their correction [2-5]. The successful solution of this task substantially defines solution quality of the subsequent tasks of the object analysis, checking, diagnostics and objects structure modification according to constraints specified by the user.

The paper is organized as follows. Types of topological faults are considered in the beginning. Further the offered technology by way of common image processing algorithms and
special inspection algorithms for processing both raster, and vector representations of topological layer is described.

1. Some topological rules

All values used during IC design should be multiple to some parameter defined as $\lambda$. This parameter is approximately equal to the maximum value of the boundary random offset of topological element, which can arise during its creation on a wafer. In addition, the required topological connectivity should not vary, even if all boundaries will be shifted separately from each other on the distances $\rho < \lambda$.

The main principles of IC topology designing were formulated by Mead and Conway for MOS ICs. Minimum width of conductor and minimum distance between conductors are basic ones for metalization layer - they should be not less than $3\lambda$. There are constraints regarded of bonding contact pads and contact windows depending on the kind of a contact (metal - metal, metal - diffusion layer, metal - polysilicon). Besides, the variety factors of manufacture technology are superimpose any additional constraints.

We shall consider ICs manufactured under MOS technology that nevertheless does not restrict of generality of the proposed algorithms.

Let's consider the following constraints for a layer:

- $D$ - minimum metal conductor width;
- $S$ - size of rectangular contact window (length of side);
- $S_1$ - distance from boundary of a contact window up to boundary of metal conductor (width of ring of a bonding contact pad);
- $K$ - size of a bonding contact pad;
- $R$ - distance from a bonding contact pad up to a metal conductor;
- $R_1$ - distance between metal conductors.

![Fig. 1 - Constraints for a layer](image)

![Fig. 2 - Constraints for neighbor layers](image)

There is only one restriction for neighbor layers: $H$ - maximum distance from centers of the same contact window.
Let's enter also a size of a minimum topology element that equals to the size of minimum detected defect:

- minimum length of a segment oriented at 0°, 45°, 90°, 135° relatively x-axis, that is considered as the extracted segment approximating a boundary of the object at this directions;
- acceptable deviation of a point from the segment, that allows to include the point into the segment.

So a problem definition is following. The raster pattern of a multi layer IC metallization as a collection of topological layers is given. Each layer is represented by a matrix of contiguous fragments partially overlapping each other. Let's consider, that the mean amount of overlapping and its acceptable deviation are known for each contiguous fragment. The set of technological rules are also given. The artwork image of a metallization can be given in addition. It is required to represent connected areas of a metallization (i.e. object) in the vector format, to fulfill check, whether obey selected object to given technological rules and to correct of the object. We shall understand a correction as an elimination of violations in the image.

2. Common algorithms of processing

Let's consider the main image processing and image analysis algorithmic stages of topology reconstruction of inspected IC:

- preprocessing of video fragments: color gamut and contrast ratio modification, anti-aliasing, noise suppression, binarisation;
- object regions (topological primitives) extraction applying raster-vector transformation, with their correction according to user parameters;
- building total object pattern from a set of object fragments, integration of object region to a single description, correction of an inter-fragment displacement;
- layers overlapping, inspection and correction of displacements of object regions for different layers;
- fragments matching in the overlapping fields.

Note that the preliminary inspection of IC is carried out at these stages. The final inspection of all design rules is carried out by the special inspection algorithms.

Let's consider in more detail each stage.

The preprocessing and binarisation include the following operations:

1) Conversion of the input image into a grayscale image with 256 intensity levels.
2) Filtering with the antialiasing purpose and noisy removal in the frequency domain.
3) Image thresholding. This stage forms the binary image where extracted object has white colour, background - black colour.
4) Enhancement of image quality by removal of blobs and aligning of boundary lines.

These operations are performed accounting design topological rules on the base of spatial filtering methods and operations of dilatation / erosion. The configuration and size of masks for spatial filters as well as amount of dilatation / erosion iterations are selected on the basis of values D, R and R1.
Extraction of object regions accounting preliminary technological rules implies the
generation of vector description of region set with the type – object / background. Straight-line
segments are used as primitives for object boundary approximation. Thus the following se-
quence of operations is performed:

1) Object contours extraction from the image. We obtain binary contour image after
execution of this operation.

2) Line extraction, approximating binary contours on the image, on the basis of Hough
transform. The preliminary accounting of technology norms: D, K, R and R1 is performed by
means of variation of Hough transform parameters such as: the orientation of the extracted
lines, minimum number of points located on the extracted line, minimum distance between
lines.

3) Cross points searching that located at the image plane. These points are "candidates"
in which direction of boundary of described object changes direction. The obtained collection
of points is converted to the set of segments located on straight lines.

4) On the base of retrieved segments creation of the set of “elementary” regions cover-
ing the initial image. Thus for every region the membership tag – object / background is in-
stalled.

5) Merging of the one-type neighboring regions into the ultimate area. As the result the
vector representation both object and background is shaped for one map by the description of
their boundaries as the ordered set of segments.

Creation of the complete map from a set of video fragments is fulfilled to obtain the
single vector description for final inspection of topological restrictions D, K, R, R1 for one
layer. At this stage fragment matching is used to find boundaries in the overlapping areas.

Overlapping of layers is an important operation both for the complete analysis of the
multi layer object. The additional complexity of this stage is cased by the fact, that layers can
have the different variants of a pasting.

Fragments matching in the overlapping fields is fulfilled both for boundaries extraction
and defects localization in the field of an overlapping. This operation allows to define
geometrical defects such as ruptures of explorers, absence of bonding contact pads, violation
of the forms of objects etc.

3. Special inspection algorithm

Algorithms allows to find out the following defects:

- ruptures of explorers;
- cross connection between explorers;
- violation of minimum width of an explorer and minimum distance between explorers;
- incorrect size and violation of a ring of bonding contact pads;
- missing or shifted contact pads.

Conclusions

The feature of proposed algorithms is:

- usage of technological rules of IC, obtained from a CAD, at different stages of processing.
from preprocessing to vectorisation;
• application of a collection of competitive algorithms of defects finding;
• post-processing of the image for defects localization.

The algorithms of image processing were tested on the task of restoring ICs metallisation topology. Thus the localization of defects was not produced, but the automatic image correction was performed. The high-quality restoring of explorers and bonding contact pads of the first layer of a metallization was reached at processing of the colour and gray-scale images with two spectral gradation.

Let's remark, that the choice of the MOS technology does not restrict usage of offered algorithms for other types of the integral technology. Besides the main algorithms can be applied not only for the analysis of metallization layers, but also other topological layers and their collection of a different type.

References


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